MITEL
SEMICONDUCTOR

MT9074
Single Chip Transceiver
Advance Information

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Features

- Combined E1 (PCM 30) and T1 (D4/ESF) framer, Line Interface Unit (LIU) and link controller with optional digital framer only mode
- LIU dynamic range of 36 dB in T1 mode; LIU dynamic range of 30 dB in E1 mode
- Two HDLCs: FDL and channel 24 in T1 mode, timeslot 0 (Sa bits) and timeslot 16 in E1 mode
- Two-frame elastic buffer in Rx & Tx (T1) directions
- Programmable transmit delay through transmit slip buffer
- Low jitter DPLL for clock generation
- Enhanced alarms, performance monitoring and error insertion functions
- Intel or Motorola non-multiplexed parallel microprocessor interface
- ST-BUS/GCI 2.048 Mbit/s backplane bus for both data and signaling
- Japan Telecom J1 Framing and Yellow Alarm
- Hardware data link access

Applications

- E1/T1 add/drop multiplexers and channel banks
- CO and PBX equipment interfaces
- Primary Rate ISDN nodes
- Digital Cross-connect Systems (DCS)

Ordering Information

MT9074AP	68 Pin PLCC
MT9074AL	100 Pin MQFP

-40°C to 85°C

Description

The MT9074 is a single chip device, operable in either T1 or E1 mode, integrating either an advanced T1 (T1 mode) or PCM 30 (E1 mode) framer with a Line Interface Unit (LIU).

The framer interfaces to a 2.048 Mbit/s backplane providing selectable data link access with optional HDLC controllers for either the FDL bits and channel 24 (T1 mode) or S_a bits and channel 16 (E1 mode). The LIU interfaces the framer to T1 (T1 mode) or PCM 30 (E1 mode) transformer-isolated four-wire line with minimal external components required.

In T1 mode the MT9074 supports D4, ESF and SLC-96 formats, meeting the latest recommendations including ITU I.431, AT&T PUB43801, TR-62411, ANSI T1.102, T1.403 and T1.408. In E1 mode the MT9074 supports the latest ITU-T Recommendations including G.703, G.704, G.706, G.732, G.775, G.796, G.823 for PCM 30, and I.431 for ISDN primary rate. It also supports ETSI ETS 300 011, ETS 300 166 and ETS 300 233.

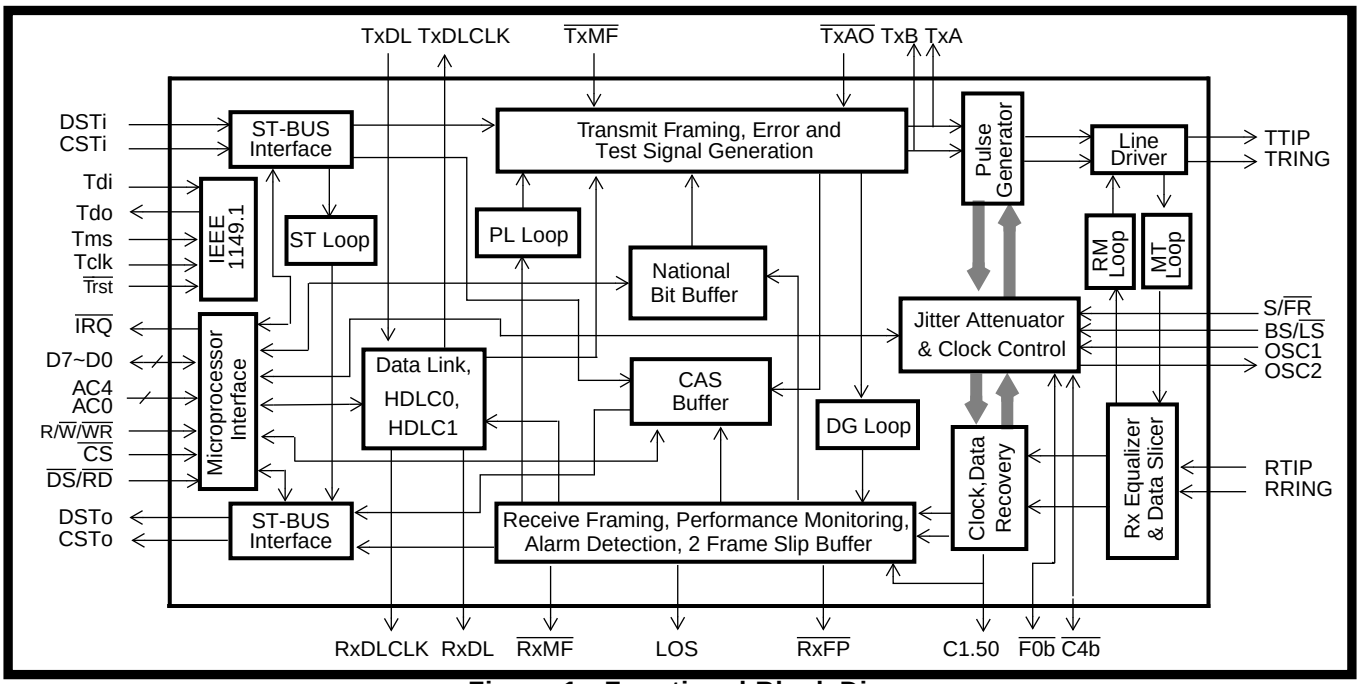
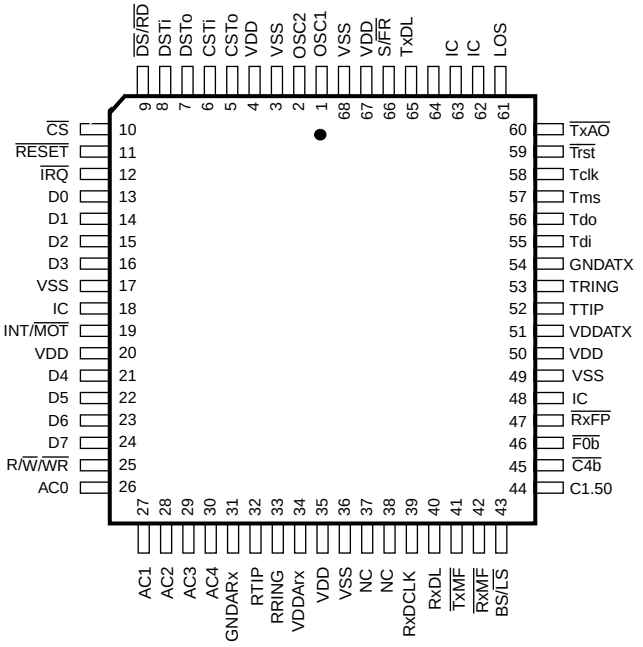
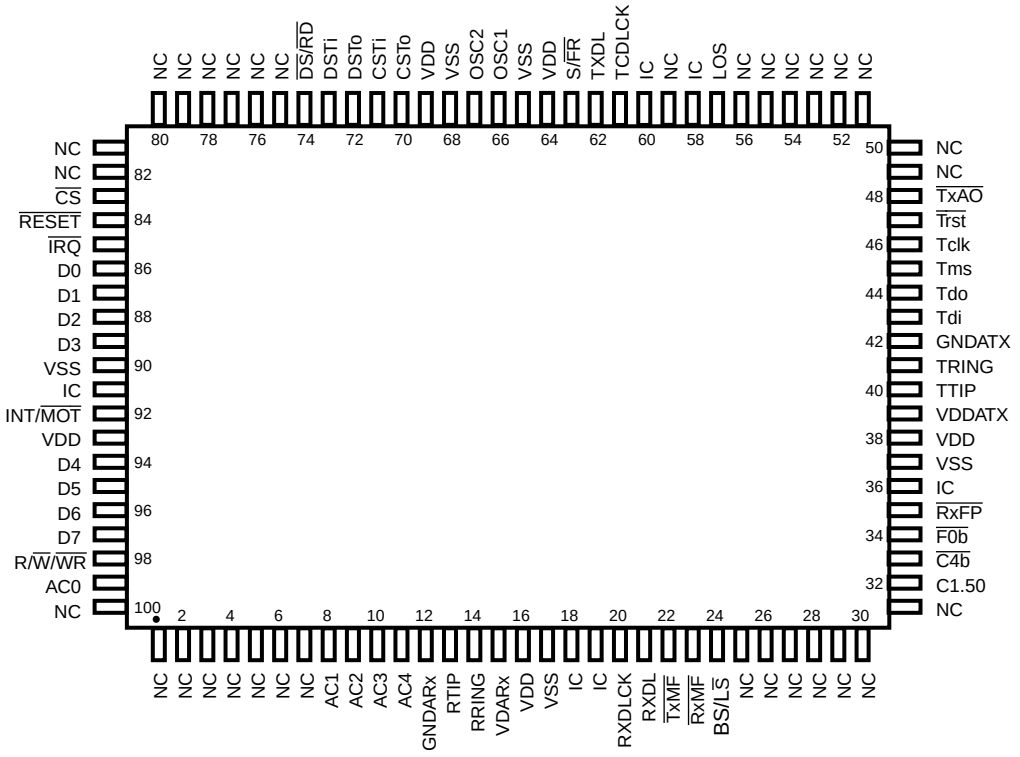


Figure 1 - Functional Block Diagram



68 PIN PLCC



100 PIN MQFP (JEDEC MO-112)

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
1	66	**OSC1**	**Oscillator Input.** This pin is either connected via a 20.000 MHz crystal to OSC2 where a crystal is used, or is directly driven when a 20.000 MHz. oscillator is employed**.**
2	67	**OSC2**	**Oscillator Output.** Connect a 20.0 MHz crystal between OSC1 and OSC2. Not suitable for driving other devices.
3	68	**V_{SS}**	**Negative Power Supply (Input).** Digital ground.
4	69	**V_{DD}**	**Positive Power Supply (Input).** Digital supply (+5V ± 5%).
5	70	**CSTo**	**Control ST-BUS Output.** CSTo carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS status stream which contains the 30 receive signalling nibbles (ABCDZZZZ or ZZZZABCD). The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are tristated when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and tristated nibbles are reversed.
6	71	**CSTi**	**Control ST-BUS Input.** CSTi carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS control stream which contains the 30 transmit signalling nibbles (ABCDXXXX or XXXXABCD) when RPSIG=0. When RPSIG=1 this pin has no function. The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are ignored when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and ignored nibbles is reversed.
7	72	**DSTo**	**Data ST-BUS Output.** A 2.048 Mbit/s serial stream which contains the 24/30 PCM(T1/E1) or data channels received on the PCM 24/30 (T1/E1) line.
8	73	**DSTi**	**Data ST-BUS Input.** A 2.048 Mbit/s serial stream which contains the 24/30 (T1/E1)PCM or data channels to be transmitted on the PCM 24/30 (T1/E1)line.
9	74	**$\overline{DS}$/$\overline{RD}$**	**Data/Read Strobe (Input)**. In Motorola mode ($\overline{DS}$), this input is the active low data strobe of the microprocessor interface. In Intel mode ($\overline{RD}$), this input is the active low read strobe of the microprocessor interface.
10	83	**$\overline{CS}$**	**Chip Select (Input)**. This active low input enables the non-multiplexed parallel microprocessor interface of the MT9074. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
11	84	**$\overline{RESET}$**	**RESET (Input).** This active low input puts the MT9074 in a reset condition. $\overline{RESET}$ should be set to high for normal operation. The MT9074 should be reset after power-up. The $\overline{RESET}$ pin must be held low for a minimum of 1µsec. to reset the device properly.
12	85	**$\overline{IRQ}$**	**Interrupt Request (Output)**. A low on this output pin indicates that an interrupt request is presented. $\overline{IRQ}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. An active low $\overline{CS}$ signal is not required for this pin to function.
13 - 16	86-89	**D0 - D3**	**Data 0 to Data 3 (Three-state I/O).** These signals combined with D4-D7 form the bidirectional data bus of the microprocessor interface (D0 is the least significant bit).

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
17	90	Vss	**Negative Power Supply (Input).** Digital ground.
18	91	IC	**Internal Connection**. Tie to Vss (ground) for normal operation.
19	92	INT/$\overline{\text{MOT}}$	**Intel/Motorola Mode Selection (Input).**A high on this pin configures the processor interface for the Intel parallel non-multiplexed bus type. A low configures the processor interface for the Motorola parallel non-multiplexed type.
20	93	VDD	**Positive Power Supply (Input).** Digital supply (+5V± 5%).
21 - 24	94-97	D4 - D7	**Data 4 to Data 7 (Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit)**.**
25	98	R/$\overline{\text{W}}$/$\overline{\text{WR}}$	Read/Write/Write Strobe (Input). In Motorola mode (R/$\overline{\text{W}}$), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{\text{W}}$ is high, the parallel processor is reading data from the MT9074. When low, the parallel processor is writing data to the MT9074.For Intel mode ($\overline{\text{WR}}$), this active low write strobe configures the data bus lines as output.
26 - 30	99, 8-11	AC0 - AC4	**Address/Control 0 to 4 (Inputs).** Address and control inputs for the non-multiplexed parallel processor interface. AC0 is the least significant input.
31	12	GND_{ARx}	**Receive Analog Ground (Input)**. Analog ground for the LIU receiver.
32 33	13 14	RTIP RRING	**Receive TIP and RING (Input)**. Differential inputs for the receive line signal - must be transformer coupled (See Figure 5).
34	15	VDD_{ARx}	**Receive Analog Power Supply (Input).** Analog supply for the LIU receiver (+5V ± 5%).
35	16	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 5%).
36	17	VSS	**Negative Power Supply (Input).** Digital ground.
37	18	TxA	**Transmit A (Output).** When the internal LIU is disabled (digital framer only mode), if control bit NRZ=1, and NRZ output data is clocked out on pin TxA with the rising edge of C1.50 (TxB has not function when NRZ format is selected). If NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail clocked out with the rising edge of C1.50.
38	19	TxB	**Transmit B (Output).** When the internal LIU is disabled and control bit NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail data clocked out with the rising edge of C1.50.
39	20	RxDLCLK	**Data Link Clock (Output)**. A gapped clock signal derived from a 2.048 Mbit/s clock, available for an external device to clock in RxDL data (at 4, 8, 12, 16 or 20 kHz) on the rising edge.
40	21	RxDL	**Receive Data Link (Output).** A 2.048 Mbit/s data stream containing received line data after HDB3 decoding. This data is clocked out with the rising edge of C1.50.
41	22	$\overline{\text{TxMF}}$	**Transmit Multiframe Boundary (Input)**. An active low input used to set the transmit multiframe boundary (CAS or CRC multiframe). The MT9074 will generate its own multiframe if this pin is held high. This input is usually pulled high for most applications.

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
42	23	**$\overline{\text{RxMF}}$**	**Receive Multiframe Boundary (Output).** An output pulse delimiting the received multiframe boundary. The next frame output on the data stream (DSTo) is basic frame zero on the T1 or PCM 30 link. In E1 mode this receive multiframe signal can be related to either the receive CRC multiframe (page 01H, address 17H, bit 6, MFSEL=1) or the receive signalling multiframe (MFSEL=0).
43	24	**BS/$\overline{\text{LS}}$**	**Bus/Line Synchronization Mode Selection (Input)**. If high, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be inputs; if low, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be outputs.
44	32	**C1.50**	**2.048 MHz in E1 mode or 1.544MHz in T1 mode, Extracted Clock (Output).** The clock extracted from the received signal and used internally to clock in data received on RTIP and RRING.
45	33	**$\overline{\text{C4b}}$**	**4.096 MHz System Clock (Input/Output).** $\overline{\text{C4b}}$ is the clock for the ST-BUS sections and transmit serial PCM data of the MT9074. In the free-run (S/$\overline{\text{FR}}$=0) or slave mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in the master mode (BS/$\overline{\text{LS}}$=1) this signal is an input clock which is phase-locked to the extracted clock (C1.50).
46	34	**$\overline{\text{F0b}}$**	**Frame Pulse (Input/Output).** This is the ST-BUS or GCI frame synchronization signal, which delimits the 32 channel frame of CSTi, CSTo, DSTi, DSTo and the PCM30 link. In the free-run (S/$\overline{\text{FR}}$=0) or slave mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in the master mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an input. The GCI/ST-BUS selection is made under software control. Page 02H, address 13H, bit 0, GCI/$\overline{\text{ST}}$=1 selects GCI frame pulse; GCI/$\overline{\text{ST}}$=0 selects ST-BUS.
47	35	**$\overline{\text{RxFP}}$**	**Receive Frame Pulse (Output).** An 8kHz pulse signal, which is low for one extracted clock period. This signal is synchronized to the receive DS1 or PCM 30 basic frame boundary.
48	36	**IC**	**Internal Connection.** Must be left open for normal operation.
49	37	**V_{SS}**	**Negative Power Supply (Input).** Digital ground.
50	38	**V_{DD}**	**Positive Power Supply (Input).** Digital supply (+5V $\pm$ 5%).
51	39	**VDD_{ATx}**	**Transmit Analog Power Supply (Input).** Analog supply for the LIU transmitter (+5V $\pm$ 5% 10%)).
52 53	40 41	**TTIP** **TRING**	**Transmit TIP and RING (Outputs).** Differential outputs for the transmit DS1 line signal - must be transformer coupled (See Figure 5).
54	42	**GND_{ATx}**	**Transmit Analog Ground (Input).** Analog ground for the LIU transmitter.
55	43	**Tdi**	**IEEE 1149.1 Test Data Input.** If not used, this pin should be pulled high.
56	44	**Tdo**	**IEEE 1149.1 Test Data Output.** If not used, this pin should be left unconnected.
57	45	**Tms**	**IEEE 1149.1 Test Mode Selection (Input).** If not used, this pin should be pulled high.
58	46	**Tclk**	**IEEE 1149.1 Test Clock Signal (Input).** If not used, this pin should be pulled high.
59	47	**$\overline{\text{Trst}}$**	**IEEE 1149.1 Reset Signal (Input).** If not used, this pin should be held low.
60	48	**$\overline{\text{TxAO}}$**	**Transmit All Ones (Input).**High - TTIP, TRING will transmit data normally. Low - TTIP, TRING will transmit an all ones signal.

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
61	57	LOS	**Loss of signal or synchronization (Output).**When high, and LOS/LOF (page 02H address 13H bit 2) is zero, this signal indicates that the receive portion of the MT9074 is either not detecting an incoming signal (bit LLOS on page 03H address 18H is one) or is detecting a loss of basic frame alignment condition (bit $\overline{\text{SYNC}}$ on page 03H address 10H is one). If LOS/LOF=1, a high on this pin indicates a loss of signal condition.
62	58	IC	**Internal Connection.** Tie to Vss (Ground) for normal operation.
	59	NC	**No Connection.** Leave open for normal operation.
63	60	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
64	61	TxDLCLK	**Transmit Data Link Clock (Output).** A gapped clock signal derived from a gated 2.048 Mbit/s clock for transmit data link at 4, 8, 12, 16 or 20 kHz. The transmit data link data (TxDL) is clocked in on the rising edge of TxDLCLK. TxDLCLK can also be used to clock DL data out of an external serial controller.
65	62	TxDL	**Transmit Data Link (Input).** An input serial stream of transmit data link data at 4, 8, 12, 16 or 20 kbit/s.
66	63	S/$\overline{\text{FR}}$/ C1.50i	**MasterSlave/Freerun Extracted Clock (Input):** If low, and the internal LIU is enabled, the MT9074 is in free run mode. Pins 45 C4b and 46 F0b are outputs generating system clocks. Slips will occur in the receive slip buffer as a result of any deviation between the MT9074's internal PLL (which is free - running) and the frequency of the incoming line data. If high, and the internal LIU is enabled, the MT9074 is in Bus or Line Synchronization mode depending on the BS/$\overline{\text{LS}}$ pin. If the internal LIU is disabled, in digital framer mode, this pin (C1.50i) takes an input clock 1.544Mhz (T1) / 2.048Mhz (E1) that clocks in the received digital data on pins RXA and RXB with its rising edge.
67	64	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 5%).
68	65	VSS	**Negative Power Supply (Input).** Digital ground.